REMARKS

Favorable reconsideration of this application, in light of the following remarks, is respectfully requested.

Claims 15-34 are pending in this application. By this Request, no claims are amended, added or cancelled.

Applicants also respectfully note that the present action does not indicate that the drawings have been accepted by the Examiner. Applicants respectfully request that the Examiner's next communication include an indication as to the acceptability of the filed drawings or as to any perceived deficiencies so that the Applicants may have a full and fair opportunity to submit appropriate amendments and/or corrections to the drawings.

Rejections under 35 U.S.C. § 103

I. Claims 15-23 and 33-34

The Examiner has rejected claims 15-23 and 33-34 under 35 U.S.C. § 103(a) as being unpatentable over Dawson et al. (U.S. Patent No. 6,229,506, hereinafter "Dawson") in view of Kimura (U.S. Publication No. 2004/0080474, hereinafter "Kimura"). Applicants respectfully traverse this rejection for the reasons detailed below.

A. Arguments relating to claims 15 and 33 (as well as their dependent claims)

The Examiner relies upon capacitor 1811 of FIG. 18A of Kimura as disclosing the "second capacitor" within the meaning of claim 15. Applicants do not agree, and submit that the capacitor 1811 of Kimura does not disclose the "second capacitor" within the meaning of claim 15. For instance, claim 15 requires that "a second capacitor, having **a first terminal** connected to the **current control terminal of the driving transistor**." In FIG. 18A of Kimura, the

Examiner asserts that the driving transistor of FIG. 18A is transistor 1809. The first terminal of capacitor 1811 is connected to the input of transistor 1809 – **not** the current control terminal of transistor 1809. Rather, the current control terminal of transistor 1809 is connected to the fourth gate signal line. Therefore, the capacitor 1811 cannot disclose the "a second capacitor, having **a first terminal** connected to the **current control terminal of the driving transistor**" because the first terminal of capacitor 1811 is connected to the input of transistor 1809, which is **not** the current control terminal of transistor 1809.

Furthermore, Dawson fails to cure the deficiencies of Kimura. For instance, referring to FIG. 3, a capacitor CC is connected to the gate of transistor P1 365. Dawson is silent on whether the transistor P1 365 is a driving transistor. Therefore, Dawson and Kimura, alone or in combination, cannot render claim 1 obvious to one of ordinary skill in the art.

Furthermore, independent claim 33 recites features similar to the above-identified feature of claim 15. For instance, claim 33 recites, *inter alia*, "by changing electric connection of the second terminal of the second capacitor from the predetermined voltage line to the current output terminal of the driving transistor by the second and third transistor." Dawson and Kimura, alone or in combination, does not render claim 33 obvious to one of ordinary skill in the art for the same reasons with respect to claim 15. Claims 16-23 and 34, dependent on independent claims 1 and 33, are patentable for at least the same reasons stated above, as well as their own merits.

B. Arguments relating to dependent claims 16 and 25

Applicants submit that FIGS. 18A-B and 19A-F of Kimura do not disclose the features of claim 16. Claim 16 recites, *inter alia*, "during a first period within a current writing period of the driving transistor, the first switching transistor connects the current control terminal to the current output terminal, the second switching transistor disconnects the second terminal and the

current output terminal from each other, and the third switching transistor connects the second terminal to the predetermined voltage line." In other words, during the first period within a current writing period, the second switching transistor may be OFF, while the third switching transistor may be ON (or vice versa). Basically, the second switching transistor is in an opposite state of the state of the third switching transistor. In other words, the second switching transistor and the third switching transistor operate in **opposite manners**.

In contrast, TFT 1818 (allegedly corresponding to the second switching transistor) and TFT 1807 (allegedly corresponding to the third switching transistor) always operate in the **same state (or same manner)** during a write period. For example, referring to FIGS. 18A-B and 19A, the second, third, and fifth gate signal lines 1803, 1804, and 1816 reach the H level and the fourth gate signal lines 1805 reaches the L level to turn the TFTs **1807**, 1808, 1809 and **1818** ON (Section 1). This generates a current as shown in FIG. 19A to charge the capacitor means 1811.

When storing of the threshold in the capacitor means 1811 is completed, the second and fifth gate signal lines reach the L level and the third gate lines reaches the H level to turn the TFTs **1807**, 1808 and **1818** OFF (section III). See Kimura, paragraph [0149] and [0151].

As a result, TFT 1818 and TFT 1807 always operate in the **same manner** in direct contrast to the requirements of claim 16.

Therefore, Kimura does not disclose "during a first period within a current writing period of the driving transistor, the first switching transistor connects the current control terminal to the current output terminal, the second switching transistor disconnects the second terminal and the current output terminal from each other, and the third switching transistor connects the second terminal to the predetermined voltage line" of claim 16. As admitted by the Examiner, Dawson does not cure the deficiencies of Kimura. Therefore, Kimura and Dawson, alone or in combination, cannot render claim 16 obvious to one of ordinary skill in the art. Also, claim 25

contains the same above-identified feature of claim 16, and therefore is patentable for the same reasons stated above.

Therefore, Applicants respectfully request this rejection to claims 24-32 under 35 U.S.C. §103(a) be withdrawn.

II. Claims 24-32

The Examiner has rejected claims 24-32 under 35 U.S.C. §103(a) as being unpatentable over Kimura in view of Dawson. Independent claim 24 recites the same above-identified feature of claim 15. For instance, claim 24 recites, *inter alia*, "a second capacitor, having a first terminal connected to the current control terminal of the driving transistor." Dawson and Kimura, alone or in combination, does not render claim 24 obvious to one of ordinary skill in the art for the same reasons with respect to claim 15. Claims 25-32, dependent on claim 24, are patentable for at least the same reasons stated above with respect to claim 15.

Therefore, Applicants respectfully request this rejection to claims 15-23 and 33-34 under 35 U.S.C. §103(a) be withdrawn.

CONCLUSION

Accordingly, in view of the above remarks, reconsideration of the objections and rejections and allowance of the pending claims in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Donald J. Daley at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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